module Imem (clk, address, instruction);

input clk;
input [7:0] address;
output [7:0] instruction;
reg [7:0] instruction;

// memAddr is an address register in the memory side.
reg [7:0] memAddr;
reg [7:0] Imem[0:512];

// Definition of the latency to latch the address and read the memory.
parameter addressLatch = 10, memDelay = 70;

// The I-Memory is initially loaded
initial
$readmemb ("Imem.data", Imem);

// I-mem is read in every cycle.
// A read signal could be added if necessary.
always @(posedge clk) begin
    #addressLatch memAddr = address;
    #memDelay instruction = Imem[memAddr];
end
endmodule