A High-Resolution Tail-Capacitor Based Tuning Scheme for LC-DCO

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Abstract—This paper presents a high resolution tuning scheme for the LC digitally-controlled-oscillator (DCO) based on desensitized tail capacitance tuning. The sensitivity of the oscillation frequency to the tail capacitance is quantitatively analyzed. The impact of the tail capacitance on the phase noise is qualitatively discussed. Our analysis and simulation results show that both the phase noise and the resolution can be improved simultaneously if the tail capacitance value is properly designed. A 2.4 GHz DCO designed in 65-nm CMOS technology is simulated for demonstration. The tuning resolution can be improved by a factor of 20, and the phase noise at 1 MHz offset can be improved by 2 dB.

Index Terms—CMOS, DCO, fine tuning resolution, phase noise, tail capacitance.

I. INTRODUCTION

With the evolution of sub-micrometer CMOS process, traditional phase-lock-loop (PLL) is being superseded by all digital phase-lock-loop (ADPLL) [1]. Digitally-controlled oscillator (DCO), with its crucial impact in phase noise and resolution, is a vital block in ADPLL. The fine resolution of DCO, along with the fine resolution of time-to-digital converter (TDC), strongly affects quantization noise introduced in the ADPLL band. However, despite the unremitting technology advancement, designing a high resolution LC-DCO in standard RF COMS technology is still challenging.

A reliable dithering technique proposed in [2] shrinks considerably the equivalent DCO frequency resolution by changing the discrete capacitance at high rate. But this still requires an intrinsic DCO resolution on a level of 10 KHz or below. Otherwise, a high order Σ∆ converter is needed to achieve a very fine frequency resolution, which will consume more area and power.

Designing a DCO with an intrinsic resolution on a level of 10 KHz is tough in practice. For instance, let us assume we design a 2.4 GHz class-B DCO with a 3nH inductor (topology is shown in Fig.1). Thus, changing only 1fF in resonator will generate a difference of about 800 KHz in output frequency. This indicates a unitary capacitance in the order of atto-Farad should be implemented. Nevertheless, a such small capacitance can be very sensitive to parasitics and troublesome in layout matching. The difference between states of a fine tuning NMOS varactor in standard RF CMOS process is often in the order of femto-Farad, which is apparently far from enough.

Popular solutions of shrinking intrinsic resolution are custom designs of the capacitive switchable components in tank [3], [4]. However, in order to fully cover the tuning range, more tuning components have to be employed by tank. All these components introduce more parasitic resistances into LC tank. This will result in a degradation of tank Q-factor, worsening the phase noise of DCO. Besides, the performance of these customized units strongly depends on the accuracy of fabrication process, which is not satisfying in reliability and robustness.

In order to solve this problem, we present a new scheme utilizing tail capacitance impacts on frequency and phase noise in class-B LC-DCO. This method needs no additional active device or customized unit, and will improve both fine tuning resolution and phase noise performance.

This paper is organized as follows: Section II discusses the impacts of tail capacitance in class-B DCO, not least in frequency and phase noise. Section III proposed a high resolution tuning scheme for DCO to verify our theory. Section IV summarized this work’s important points.

II. THE ROLE OF TAIL CAPACITANCE IN CLASS-B DCO

Prior to proposing our new topology, we want to discuss the impact of tail capacitance $C_{tail}$ in class-B DCO on frequency resolution and phase noise. The theoretical analysis will provide insight to our design.

A. Diminution Effects of the Capacitance in Tail

The classical class-B DCO topology is shown in Fig.1. For convenience of the capacitance analysis, we divide an oscillation period into three intervals according to the working status of cross-coupled pair $M_1/M_2$ (shown in Fig.2.(d)). The first interval, as shown in Fig.2 (a), is when the differential
The effective impedance across the tank, the equivalent circuits during to-back saturated device are [6]

\[ Z_2 = \frac{2g_{m} + 4sC_{gs} + 2sC_{tail}}{4s^2C_{gs}^2 + 2s^2C_{gs}C_{tail} - sC_{tail}g_{m}} \]  

Assuming \( C_{gs} \) and \( C_{tail} \) is small, from (7) we can get an equivalent capacitance as

\[ C_2 \approx \frac{C_{tail}}{2} \]  

Thus, \( \Delta C_2 \approx -\Delta C_{tail}/2 \). Similarly, from (8), we can get

\[ \Delta C_3 \approx \left(\frac{1}{2} + \frac{g_{m,M_2,R}}{g_{m,M_2,L}}\right) \Delta C_{tail} \]  

At the peak amplitude, the triode device will behave like a short circuit resulting in \( g_{m,M_2,R} = g_{m,M_2,L} \), which leads to \( \Delta C_3 = \Delta C_{tail}/2 \). The frequency change by DCO tail capacitance can be denoted as

\[ \frac{\Delta f}{f_0} \approx \frac{\Delta C_{eq}}{2C_{tank}} \]  

where \( \Delta C_{eq} \) is periodic average of \( \Delta C_1, \Delta C_2 \) and \( \Delta C_3 \). Recalling that \( \Delta C_1 \approx 0 \) and \( \Delta C_2 \approx -\Delta C_{tail}/2 \), we can conclude that the effective tail capacitance variation in resonator will be remarkably diminished, which leads to the frequency desensitization.

Although the above analysis based on small-signal models may not sufficiently predict the large-signal behavior of an oscillator, it still provides insight and theoretical base for our design.

**B. Impacts on Phase Noise**

The tail current source \( M_0 \) in class-B LC oscillator often has a much larger size than cross-coupled pair \( M_1/M_2 \). Even if we do not design \( C_{tail} \) intentionally, this large \( M_0 \) will introduce a large tail parasitic capacitance \( C_{par} \). For instance, \( C_{par} \) is usually between 0.5 pF to 1 pF under 90-nm CMOS [7]. This \( C_{par} \) affects noise current behaviours of both tail current source and differential pair. Thus, our following discussions applies to all LC-oscillators in classical class-B topology.
Fig. 3. Impacts of tail capacitance in LC-DCO phase noise during (a) \((-\phi_1, \phi_1)\) and (b) other time in a period.

During \((-\phi_1, \phi_1)\) defined in (2), the noise current flows are shown in Fig.3 (a). The tank noise injected from the tail current through \(M_1\) and \(M_2\) are relevant, and they will cancel each other at the differential output in oscillator after going through two paths. Thereupon, the tail current source contribute very little noise during this time, even without \(C_{\text{tail}}\). The noise current (at \(\omega_0 \pm \Delta \omega\)) of cross-coupled pair, however, will inject into tank directly generating phase noise during this interval. Even if some of noise charges of \(M_2\) may charge onto \(C_{\text{tail}}\), the discharging amount of noise charges which transfer from \(C_{\text{tail}}\) to \(M_1\) will counteract this effect. Thus, the existence of \(C_{\text{tail}}\) has little influence in \((-\phi_1, \phi_1)\).

When only one branch of the differential pair is on, the noise current flows are shown in Fig.3(b). Assuming the active one is \(M_2\), the tail current MOSFET \(M_0\) and \(M_2\) just work like the cascode topology [5]. The tail capacitance forms a path for noise current \(i_{\text{2n,M2}}^\text{2}\) from LC-tank to ground. That is to say, \(C_{\text{tail}}\) impairs the cascode effect which will increase the noise contribution of \(M_1/M_2\). However, this low impedance path to ground formed by \(C_{\text{tail}}\) also diminishes the portion of \(i_{\text{2n,tail}}^\text{2}\) injected to tank. Therefore, it can be seen that \(C_{\text{tail}}\) is friendly to us for tail current noise but bad for cross-coupled pair noise.

Furthermore, if properly designed, the tail capacitance can also enlarge the amplitude while keeping the power dissipation constant, which lead to a better phase noise performance. Actually, by adding a relatively large tail capacitance, the current efficiency can be enhanced by one third [8].

With the discussions above, we can conclude that a trade-off in designing \(C_{\text{tail}}\) truly exists when concerning phase noise, and there must be an optimal point for its value. In Section III, we will find this optimal point.

III. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The proposed DCO fine tuning scheme is shown in Fig.4. A 2.4 GHz DCO is designed in standard 65-nm CMOS RF technology for demonstration. A 1nH inductor in the thick-metal layer with a \(Q\) factor of 19 is used in \(LC\) tank. The binary coarse tuning tank is designed with MIM capacitances. A fixed capacitance \(C_{\text{fixed}}\) is placed parallel to tail current source \(M_0\). The total tail capacitance \(C_{\text{tail}} = C_{\text{par}} + C_{\text{fixed}} + C_{\text{fine}}\). By properly choosing the value of \(C_{\text{fixed}}\), \(C_{\text{tail}}\) can be designed to ensure its value is around the optimal point of phase noise. To find this optimal point, spectreRF simulations on phase noise were run by sweeping the capacitance with a 200 fF step. The results are shown in Fig.5. It can be seen the optimal point is around 1 pF, which also verified our theory in Section II reciprocally. A 2 dB phase noise improvement can be achieved by this technique. Thus, we choose the \(C_{\text{fixed}} = 1\) pF to ensure our oscillator has a good phase noise performance.

Fig. 4. Proposed DCO topology with a tail fine tuning bank.

Fig. 5. Simulation results in optimizing \(C_{\text{fixed}}\) for phase noise.

Fig. 6. Fine tuning tank.
TABLE I
SUMMARY RESULTS AND COMPARISON WITH STATE-OF-THE-ART

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<tr>
<th></th>
<th>This work</th>
<th>[9]</th>
<th>[3]</th>
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<td>Center Freq. (GHz)</td>
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<td>5.8</td>
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<td>Tuning Range (GHz)</td>
<td>0.54 (24%)</td>
<td>0.78(26%)</td>
<td>0.62(11%)</td>
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<tr>
<td>Coarse Freq. Resolution (MHz)</td>
<td>1.5</td>
<td></td>
<td>2.4</td>
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<tr>
<td>Fine Tuning Range (MHz)</td>
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<td>2~12</td>
<td>2.75</td>
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<tr>
<td>Fine Tuning Resolution (KHz)</td>
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<td>0.15~1.5</td>
<td>14</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
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<td>28.8</td>
<td>9.2</td>
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<tr>
<td>Phase Noise@1MHz (dBc/Hz)</td>
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<td>-117.6</td>
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<td></td>
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<td>183</td>
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<tr>
<td>CMOS Technology</td>
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</table>

1 Post-simulation results.

We implement the fine tuning capacitance tank with a $8 \times 16$ varactor matrix. The schematic is shown as Fig.6. Naturally, each fine tuning unit has about a 1fF difference between connection to $V_{DD}$ and $Gnd$. From post-simulation results, the total fine tuning range is 2 MHz which can cover the coarse frequency resolution. According to (11), the $\Delta C_{eq}$ of each tuning unit is about 50 aF, which has been improved by a factor of 20. This also substantiates our deduction.

The final layout of our DCO core and phase noise simulation result are shown in Fig.7 and Fig.8, respectively. The summary of performance is given in TABLE I, from which we can see our design is comparable to state-of-the-art in all aspects.

IV. CONCLUSION

This article has presented a high resolution tuning scheme for LC-DCO, which is based on desensitized tail capacitance tuning. The sensitivity of the oscillation frequency to the tail capacitance is quantitatively analyzed. The impact of the tail capacitance on the phase noise is qualitative discussed. Our analysis and simulation results show that both the phase noise and the resolution can be improved simultaneously if the tail capacitor value is properly designed. A 2.4 GHz DCO designed in 65-nm technology is simulated for demonstration. The tuning resolution can be improved by a factor of 20, and the phase noise at 1 MHz offset can be improved by 2 dB.

ACKNOWLEDGMENT

This work was partly supported by National Natural Science Foundation of China, under Grant 61204033. The authors would like to thank Mr. S. Diao at East China Normal University, Shanghai, China, Dr. N. Chen, at Kunming Institute of Physics, Yunnan, China, and Mr. L. Wu at ETH Zurich, Zurich, Switzerland for helpful discussions and suggestions. They are also grateful for the support by the Information Laboratory Center of USTC on EDA tools, and they would also like to acknowledge MediaTek for USTC students and project sponsorship.

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