

SAHIL ASHOK DEORA

1234 West 37th Pl, Apt 2, Los Angeles, CA 90007 | 1-716-867-4440 | sdeora@usc.edu | <http://www-scf.usc.edu/~sdeora/>

EDUCATION:

UNIVERSITY OF SOUTHERN CALIFORNIA, Los Angeles, CA Expected Graduation May 11
M.S. Electrical Engineering (focus in Analog & VLSI Design)
UNIVERSITY AT BUFFALO, STATE UNIVERSITY OF NEW YORK, Buffalo, NY June 09
B.S. Electrical Engineering | Magna cum Laude | Engineering Distinction

SKILLS:

Programming Languages: HTML, UNIX, SQL, ARM & Harvard Architecture, C, C++, Java, VHDL, Verilog, SKILL
Tools: Cadence - Virtuoso, Schematic Editor & NC Verilog, Synopsys - Custom Designer, Design Compiler & WaveView, Magic, SPICE, Spectre, HSPICE, hspice-S, hspice-D, JEeye II, LTspice, Eclipse, Allegro, LabView, Altera Quartus II, Aldec Active-HDL, PADS Layout, Maple, MS Office 2003/2007 Suite, Adobe Dreamweaver & Photoshop, FoxPro, Metrowerks CodeWarrior IDE, wspice3, OrCAD PSpice
Engineering Related: Soldering surface mount components, Programmable Logic Control (PLC), & experience with standard lab equipment such as oscillators, spectrum analyzers, network analyzer, function generators, AFM, STM.

TECHNICAL EXPERIENCE:

INPHI CORPORATION

Signal Integrity Intern, Westlake Village, CA, USA May 10 – Aug 10

- Tested & developed GUI test benches based on HSPICE models for signal integrity parameterized (p)-cells
 - Identified bugs & coordinated with Vendor for solutions
- Performed Statistical Eye Analysis, simulated Eye Diagrams & Jitters for test benches using JEeye & WaveView
 - Compared & reported - simulated eye diagrams & real simulations

MAXIM INTEGRATED PRODUCTS

Power & Battery Management Technical Intern, Sunnyvale, CA, USA June 08 – Aug 08

- Researched & individually worked on Light Modulation Unit for portable devices using Harvard Assembly language
- Researched, obtained & reviewed typical operating characteristics (TOCs) for future products

NOVATIUM

Project Development Engineering Intern, Chennai, India July 07 – Aug 07

- Fabricated PC board with reduced electrical components
- Collaborated with the project development team to test & debug different versions of their products

GDA TECHNOLOGIES INC.

Summer Engineering Intern, Chennai, India July 06

- Created various models of electrical circuits on OrCAD PSpice & Allegro & ran simulations for fabrication

LEADERSHIP EXPERIENCE:

STUDENT SUPERVISOR, ITS, University of Southern California, Los Angeles, CA, USA Oct 09 – Present

- Performing duties & supervising over 60 student operators across 3 public computing centers at USC

TEACHING ASSISTANT, Electrical Engineering Dept., University at Buffalo, Buffalo, NY, USA Aug 08 – May 09

- Mentored & monitored over 200 students across 3 Undergraduate Engineering courses on labs & recitations

RESIDENT ADVISOR, University Residence Halls, University at Buffalo, Buffalo, NY, USA Aug 07 – May 08

- Personally supervised & monitored the health & well-being of 40 residents. Have emergency preparedness training.
- Organized various social & educational based programs for residents on campus throughout the year.

PROJECTS:

VLSI SYSTEMS & DESIGN

- Performing architectural design & analysis, Verilog implementation, simulations for design verification for DDR2 SDRAM memory controller
- Designed 32 & 16-bit Multipliers & Adders such as Static, Dominic, Ripple Carry, Carry Select, Carry Look-up, 32-word, 8-bit Content addressable memory (CAM) & compared 3 different types of commercially available CAM designs on a pad-frame of 900*900 μm^2 using CADENCE Virtuoso AMI 0.6 μm Technology.

ANALOG DESIGN

- Designed several low-voltage & power, high-speed & gain Operational on LTspice, Cadence Tools, Magic, SPICE & integrated on MOSIS. Used TSMC 180nm & AMI 1.5 μm technology

VLSI TESTING

- Designed 32 bit Pseudo random pattern generator (PRPG) using Verilog & CAD tools
- Performed Test Logic Synthesis, Test Generations, Encounter Test on an 8-bit RISC Microcontroller (ALU) using RTL Compiler & Cadence tools

AWARDS: Awarded \$10000 International Academic Scholarship, Awarded Dean's List, & placed first in a Tennis Competition

ACTIVITIES/INTERESTS:

Member of USC Anjaane & UB Jalwa Indian Fusion dance team, IEEE, Eta Kappa Nu Honor Society, USC Entrepreneur Club, Association of Indian Student (AIS), UB Aces Tennis Club, Volleyball, Tennis & Racquetball Intramurals team