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SUMMARY

Computer scientist and experienced cellular System on Chip(SoC) software architect with an entrepreneurial spirit. Experienced technology leader with strong skills in leading cross-functional teams, managing end-to-end product lifecycle, justifying new product features, determining and documenting new requirements, maintaining the conceptual integrity of the product and feature set, writing technology specifications and launching new products to the marketplace both as development and stability commercialization lead. Proven track record in problem solving: developed a core set of tools, techniques and knowledge base to debug any issue when handed a 'dead' phone, the first such knowledge base for industry's first dual processor cellular system.

GRADUATE SCHOOL

University of Southern California *Los Angeles, CA*
PhD Candidate in Artificial Intelligence and autonomous agents ***Jan 2014 – May 2017***

Building the first spoken language processing capability in a cognitive architecture by blending breakthroughs in machine learning with classical symbolic AI. This project is an integrative, system building approach to AI that involves leveraging graphical models – factor graphs – to design efficient inference strategies for spoken language processing in a manner that is consistent with how knowledge is processed in every aspect (vision, reasoning, decision making etc.) of the system – a novelty for spoken language processing. The project aims to serve as a first step towards developing a full-fledged theory of human language processing that is grounded in cognitive architectures and uses consistent representations across all capabilities. Selected publications:

- Journal Paper '*Continuous phone recognition in the Sigma cognitive architecture*' presented at the Biologically Inspired Cognitive Architectures conference (BICA), 2016, at The New School of Design, NY.
- Journal Paper '*Isolated word recognition in the Sigma cognitive architecture*' presented at the Biologically Inspired Cognitive Architectures conference (BICA), 2014, at MIT.

PROFESSIONAL EXPERIENCE

Qualcomm Inc., *San Diego, CA*
Modem ASIC Software Architect, Platform Architecture ***Jan 2013 – Jan 2014***

Drove reconciliation of market requirements with Qualcomm's chipset roadmap. Responsibilities included, but not limited to maintaining conceptual integrity of product features by interfacing with product managers and technology development heads. This consisted of understanding product needs, planning & prioritizing cross-functional feature deliverables with team leads by driving consensus on – at times – conflicting technology needs of the solution and delivery schedules. Took part in a 7-day leadership and negotiations training by the *Harvard Negotiations Project* for product architects.

- Led a cross-functional effort consisting of 6 Principal engineers to define unified cellular, GPS, WiFi power architecture on a new tier of modem chips, an estimated $200M+ market.
- Spearheaded and evangelized proof of concept to leverage modem hardware to automate software fault analysis. Proposed plan to reduce customer issue turn-around time by 25%.
- Led a team of staff and Sr. staff engineers to develop set of core software strategies to reduce modem software development time by mitigating hardware change impact on modem software. Proposed strategies would reduce development time by up to 33%.
- Led a team to strategize measuring crypto block's performance on ARM Trustzone boot.

Modem ASIC DSP Staff Software Engineer ***April 2011 – Dec 2012***

Responsibilities included development and management of software development teams of up to 6 senior engineers. Requirement negotiations, wireless protocol design and development.

- Built and managed the LTE Firmware group of 4 senior engineers for the wireless LAN/Bluetooth coexistence module. The coexistence module I developed was regularly sourced across 6 product lines.
- Managed the WCDMA to LTE Mobility feature development group of 6 senior engineers, driving consensus amongst multiple protocol software and firmware teams.

- Set FW SCRUM sprint deadlines and held SCRUM meetings to present status to management.
- Improved existing systems algorithms by eliminating overhead to achieve savings of up to 20%.
- Developed a generic SCRUM template to aid SW program managers derive specific templates.

- Developed the memory overlay feature to enhance memory usage by 30%.

Modem ASIC Senior Software Engineer ***August 2007 – March 2011***

- Developed and commercialized LTE Physical Layer connected mode searcher responsible for maintaining cellular calls under mobility the conditions. Led subsequent industry leading feature commercialization for the LTE air interface physical layer.
  - Developed key optimizations to improve reporting accuracy & achieving power saving of 10%.
- Led for the first proprietary multiprocessor communication driver module to enable multicore architecture of LTE modem. Improved on open standard reference driver by 23% in terms of speed.
- Architected and developed inter-processor shared memory 'Diagnostics' solution to unblock Corporate R&D's first LTE prototype.
- Developed connected mode searcher to achieve Corporate R&D's first LTE handover.
- Ported and performed silicon 'bringup 'of CR&D Physical Layer implementation to be POSIX compliant.

Modem ASIC Software Engineer ***Jan 2005 – July 2007***

- Built and led the cross-functional 'stability' triage team of 4 engineers to handle cellular industry's first dual processor chipset**.**
  - Stability team commercialized two product lines, including industry's first dual processor Windows phone.
  - Debugged several complex issues involving multiple modules in a multicore environment with multiple Operating Systems, including Windows Mobile, REX, Qube, L4.
- Led several Qualcomm RTOS (REX, Qube, BLAST) 'bringups' on various chipsets and RUMI emulation.
- Developed QCT's first Serial Peripheral Interface (SPI) Hardware Abstraction Layer (HAL) and device driver.
  - HAL development mitigated hardware interface changes in downstream targets by 15%
- Developed Boot ROM reset protocol for Qualcomm's Thunderbird target.
- Added debug capability to modem Heap Manager to detect memory leaks.

Wipro Technologies Inc., *Pune, India*

Systems Software Engineer ***September 2000 – December 2002***

- WCDMA RRC Layer development – developed RRC connection establishment procedure.
- Set formal C coding guidelines for Wipro Telecom division in Pune.

SKILLS

DEVELOPMENT – C/LISP/PYTHON/JAVA/C++/ARM ASSEMBLY/OPEN CL/BASH

TOOLKITS – MATLAB/TENSORFLOW/HTK/GMTK/THEANO/KERAS

TOOLS – PERFORCE/GIT

TECHNOLOGIES – POSIX/MPI/VLIW INSTRUCTION SET ARCHITECTURE/DSP/FIXED WIDTH PROGRAMMING/TRACE 32/DEEP LEARNING/SPEECH PROCESSING/NATURAL LANGUAGE PROCESSING/MACHINE LEARNING

EDUCATION

UNIVERSITY OF SOUTHERN CALIFORNIA *Los Angeles, CA*

PHD, ARTIFICIAL INTELLIGENCE (CS) ***JAN 2014 – MAY 2017***

UNIVERSITY OF SOUTHERN CALIFORNIA *Los Angeles, CA*

MS (CS) ***JAN 2003 – DEC 2004***

UNIVERSITY OF PUNE *Pune, India*

BE (ELECTRONICS & TELECOMMUNICATIONS) ***JUN 1996 – JUN 2000***