

JOSEPH RODERICK ROBINSON HAULE

10368 1/2 Bellwood Ave. • Los Angeles, California 90064 • 512.694.9501 • haule@usc.edu

EDUCATION

Master of Science, Electrical Engineering, December 2007

The University of Southern California

Overall GPA: 3.28/4.00

Bachelor of Science, Electrical Engineering, August 2004

The University of Texas at Austin

Overall GPA: 3.00/4.00

EXPERIENCE

Intel Corporation, Intern Hardware Engineer, Platform Validation Engineering (01/07 – 07/07)

- Researched and successfully configured BitLocker, the initial component to Trusted Platform Management testing, in Folsom Platform Validation Engineering Lab
- Authored software automation scripts for Intel® VPRO installation and GFX testing, minimizing the time required to validate these features and insuring validation was performed consistently at various sites
- Performed Intel® VPRO validation on the Crestline mobile platform, and contributed to getting Crestline PRQ'd on time

Intel Americas, Extern Sales Associate, Intel Business Sales (09/06 – 12/06)

- Successfully launched Core® 2 Duo Processor products at Los Angeles area Best Buy stores
- Increased awareness of Core® 2 Duo Processor Products and Centrino® Duo Mobile Technology by completing in-store trainings at Best Buy
- Increased Intel's merchandising presence in Best Buy Torrance, Hawthorne, West Los Angeles, and Culver City

Intel Corporation, Intern Software Engineer, Platform Application Engineering (01/06 – 08/06)

- Owned test execution for critical BIOS compliance test at Intel® AMT and platform workshops
- Responsible for implementing test systems for exploration and debugging of Kerberos Network Authentication Protocol
- Contributed to BAT execution and owned BAT execution for Intel® AMT software on HP Maverick and Lenovo platforms
- Awarded 3 department awards

IBM, Intern Pre-Professional Engineer, Systems Test Integration (06/04 – 12/04)

- Re-designed processor nest manufacturing process, which contributed to minimizing the time needed to manufacture and test ERIF5 validation tools
- Assisted in manufacturing, debugging, and packaging of ERIF5 tools
- Contributed to re-factoring of software application from Pearl to Java, which minimized code size of original application

IBM, Intern Pre-Professional Engineer, Global Systems Integration (01/03 – 12/03)

- Researched, designed and implemented test plans for testing midrange Regatta servers
- HW bring-up and debug engineer for IBM Squadrons Servers, follow-on to Regatta

IBM, Intern Pre-Professional Engineer, ERIF Development (01/02 – 08/02)

- Authored LabView drivers for evaluation and integration of power supplies for Si-validation tester, which contributed to minimizing the cost of ERIF tools
- Si-validation, contributed to stress analysis and characterization of various Power5 Processors

USC PROJECTS

Integrated Circuit Fabrication Process (08/07 – 12/07)

- Individual project, using fabrication tools in a clean room environment to create ICs
- Performed all fabrication steps to create working IC
- Characterized IC

An Eclipse Plug-in for Use-case Authoring (08/06 – 05/07)

- Team project, primary author of System Software Requirements document and Operational Concept Description
- Maintained project website and CVS repository

Socket Programming Server Environment (05/05 – 08/05)

- Researched socket fundamentals and created real-time server environment to perform math computations in C language

TECHNICAL ABILITIES

Software Knowledge: Programming languages known: Assembly and C / Professional experience in writing LabView Drivers / Software application packages (Office Suite, Dreamweaver) / Ability to function in Mac, Unix (Linux) and Windows operating systems / HTML design, including website administration and deployment