

# Cadence Tutorial 7

## Generating HSPICE Netlist from Schematic

### EE577b Fall 98

In this tutorial, I will show how to generate HSPICE netlist from schematic.

#### 1. Tutorial Setup

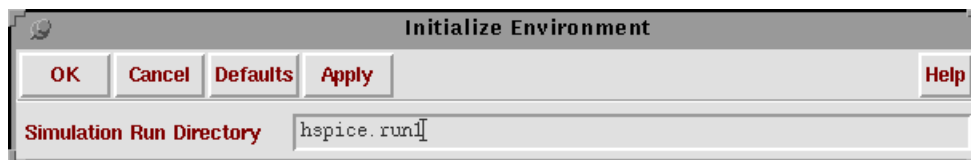
Tutorial 1,2,4 are necessary to start this tutorial.

#### 2. Open adder8 Schematic

As usual!!

#### 3. Initiate Netlist Generation Tool

1. sch:Tools->Other
2. sch:Simulation->Initialize  
Initialize Environment form will be displayed.



3. Type *hspice.run1* or use default (*spice.run1*) in **Simulation Run Directory**
4. Click OK.

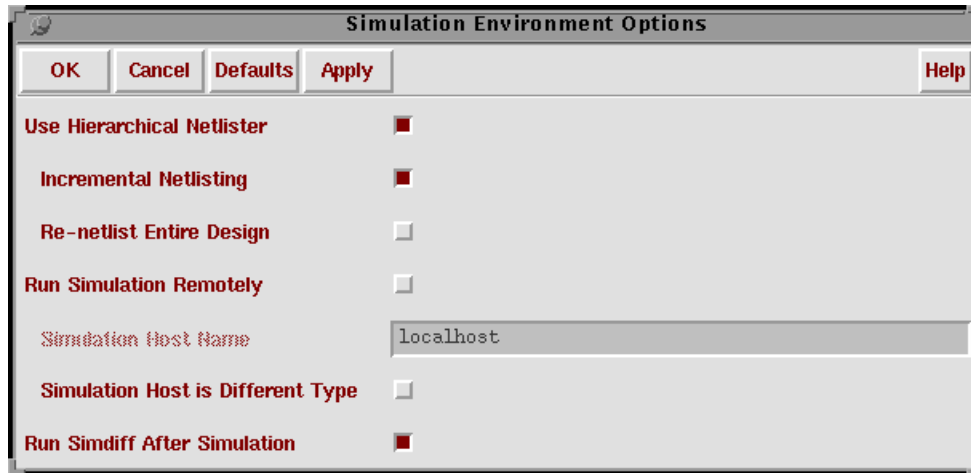
Initialize Environment form will be displayed.



5. Choose *hspice* for **Simulator Name**
6. Use default for others.
7. Click OK.

## 4. Choose Option

1. sch:Simulation->Option
2. Simulation Environment Options form will be displayed.
  - Click **Use Hierarchical Netlister** option if you want hierarchical netlist which includes all sub blocks as sub circuits call. If you want flat hspice netlist, leave it unselected.
  - We don't run hspice simulation directly from cadence tools so other options regarding simulation are not important.
  - Use **Incremental Netlisting** because it can reduce execution time for netlisting.
  - I will choose **Hierarchical Netlister**.
  - Click OK.



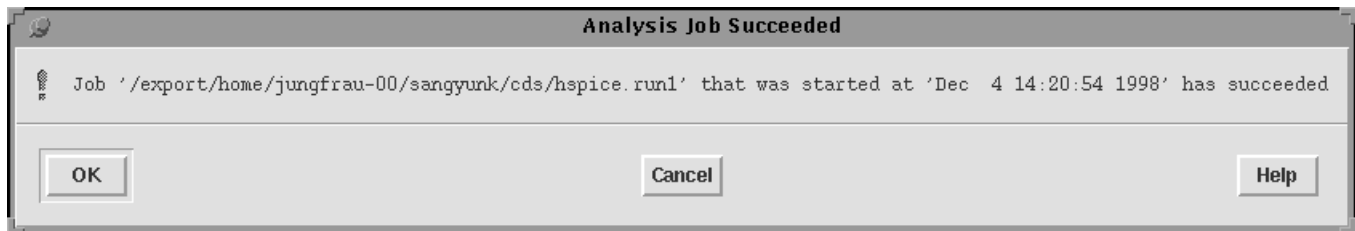
## 5. Start Netlisting

1. sch:Simulation-> Netlist/Simulate
2. Netlist and Simulate form will be displayed.
3. Turn off **Simulate** option in **Run Actions**.
4. Click OK.



## 6. Check Output

1. If there is no problem, you will get the following window saying your netlist is generated successfully.



2. In your *hspice.run1* directory, you will get *netlist* file as follows.

```

$*****
$ HSPICE Netlist:
$
$ Block: adder8
$ Netlist Time: Dec 4 14:21:05 1998
$*****

$*****
$ GLOBAL Net Declarations
$*****
.global vdd gnd

$*****
$ MODEL Declarations
$*****
.model nmos nmos level=2 vto=0.7 gamma=0.2 kp=3e-05 lambda=3e-07 tox=6e-07
.model pmos pmos level=2 vto=-0.7 gamma=0.4 kp=1.5e-05 lambda=0.3 tox=6e-07

$*****
$ Sub-Circuit Netlist:
$
$ Block: inverter
$ Last Time Saved: Nov 16 16:01:31 1998
$*****
.subckt inverter a x nl=2 nw=3 pl=2 pw=8
mxp0 x a vdd vdd pmos w=pw l=pl
mxn0 x a gnd gnd nmos w=nw l=nl
.ends inverter

$*****
$ Sub-Circuit Netlist:
$
$ Block: nor2
$ Last Time Saved: Nov 16 19:42:44 1998
$*****

```

```
.subckt nor2 a b x pl=2 pw=16 nl=2 nw=3
mxn1 x b gnd gnd nmos w=nw l=nl
mxn0 x a gnd gnd nmos w=nw l=nl
mxp1 x b net38 vdd pmos w=pw l=pl
mxp0 net38 a vdd vdd pmos w=pw l=pl
.ends nor2
```

```
*****
$ Sub-Circuit Netlist:
$
$ Block: nand2
$ Last Time Saved: Nov 16 19:45:07 1998
*****
.subckt nand2 a b x pl=2 pw=8 nl=2 nw=6
mxn1 net6 b gnd gnd nmos w=nw l=nl
mxn0 x a net6 gnd nmos w=nw l=nl
mxp1 x b vdd vdd pmos w=pw l=pl
mxp0 x a vdd vdd pmos w=pw l=pl
.ends nand2
```

```
*****
$ Sub-Circuit Netlist:
$
$ Block: half_adder
$ Last Time Saved: Dec 2 13:39:21 1998
$ Sub-Circuit Netlist:
$
$ Block: nor2
$ Last Time Saved: Nov 16 19:42:44 1998
*****
.subckt nor2 a b x pl=2 pw=16 nl=2 nw=3
mxn1 x b gnd gnd nmos w=nw l=nl
mxn0 x a gnd gnd nmos w=nw l=nl
mxp1 x b net38 vdd pmos w=pw l=pl
mxp0 net38 a vdd vdd pmos w=pw l=pl
.ends nor2
```

```
*****
$ Sub-Circuit Netlist:
$
$ Block: nand2
$ Last Time Saved: Nov 16 19:45:07 1998
*****
.subckt nand2 a b x pl=2 pw=8 nl=2 nw=6
mxn1 net6 b gnd gnd nmos w=nw l=nl
mxn0 x a net6 gnd nmos w=nw l=nl
mxp1 x b vdd vdd pmos w=pw l=pl
mxp0 x a vdd vdd pmos w=pw l=pl
.ends nand2
```

```

$*****
$ Sub-Circuit Netlist:
$
$ Block: half_adder
$ Last Time Saved: Dec  2 13:39:21 1998
$*****
.subckt adder8@sheet002 a7 a6 a5 a4 a3 a2 a1 a0 b7 b6 b5 b4 b3 b2 b1 b0 c3
+cout s7 s6 s5 s4 s3 s2 s1 s0
xi0 b4 a4 c3 net11 s4 full_adder
xi1 b5 a5 net11 net16 s5 full_adder
xi2 b6 a6 net16 net21 s6 full_adder
xi3 b7 a7 net21 cout s7 full_adder
.ends adder8@sheet002

$*****
$ Sub-Circuit Netlist:
$
$ Block: adder8@sheet001
$ Last Time Saved: Dec  2 13:39:08 1998
$*****
.subckt adder8@sheet001 a7 a6 a5 a4 a3 a2 a1 a0 b7 b6 b5 b4 b3 b2 b1 b0 c3 cin
+s3 s2 s1 s0
xi3 b3 a3 net1 c3 s3 full_adder
xi2 b2 a2 net15 net1 s2 full_adder
xi1 b1 a1 net20 net15 s1 full_adder
xi0 b0 a0 cin net20 s0 full_adder
.ends adder8@sheet001

$*****
$ Main Circuit Netlist:
$
$ Block: adder8
$ Last Time Saved: Dec  2 13:39:38 1998
$*****
xsh2 a7 a6 a5 a4 a3 a2 a1 a0 b7 b6 b5 b4 b3 b2 b1 b0 c3 cout s7 s6 s5 s4 s3 s2
+s1 s0 adder8@sheet002
xsh1 a7 a6 a5 a4 a3 a2 a1 a0 b7 b6 b5 b4 b3 b2 b1 b0 c3 cin s3 s2 s1 s0
+adder8@sheet001

```

3. If you fail to get netlist, see the background output log by selecting  
sch:Simulation->Show Outputs->Show Run Log->Show Background Run log

## 6. Run HSPICE

1. Delete model definition inside *netlist* file (bold type specified above)
2. Create *adder8.cir* file with the following lines and stimulus.

```

.include 'netlist'
.include '~ee577/cad/lib/spice/hp14b.spice'

```

Good Luck!!