Cadence Tutorial 5

Comparing Verilog-XL Simulation

EE577b Fall 98

In this tutorial, you are going to compare the simulation results from the two previous simulation results. Recall that the same stimulus was used in each.

1. Tutorial Setup

1. Finish the cadence tutorial 3, 4 before you start this tutorial.
2. Invoke “icds”.

2. Open the Verilog-XL Integration Environment

1. In the adder8 schematic window, initialize the Verilog-XL integration with the run directory of *adder8.run2*.

3. Comparing Simulation Results

1. In the Verilog-XL integration window, select
Debug->Utilities->SimCompare.
The simulation Comparison form is displayed.
2. In the Simulation Comparison form, enter the following values.

Golden Run Directory	~/cds/adder8.run1
Finish Time	300000
Cycle Time	20
Strobe Offset	15
Strobe Width	4
Tolerance	2
Report Verbosity Level	Summary

Disable SimWave option because we cannot use SimWave at this time.
For the meaning of each item, please refer 6-31 of handout by Cadence.
3. Click on OK
After while, SimCompare Report will appear to say “No mismatches”.

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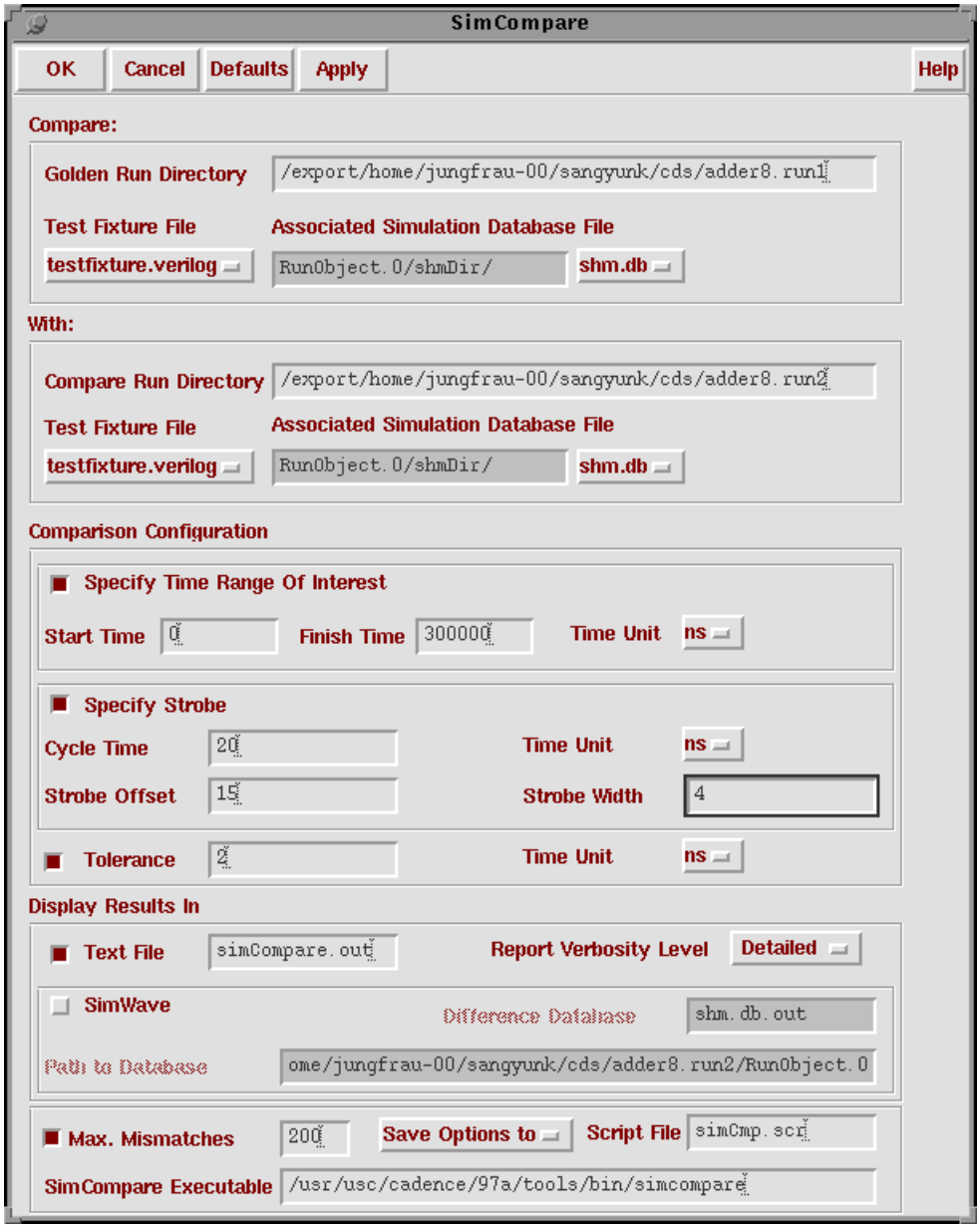
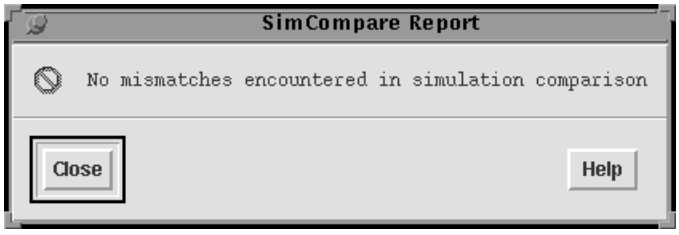
Click Close.





4. How to debug

In this tutorial, we don't have any mismatch. However, if there is any mismatch bewteen two designs, you will get simCompare.out file in your *adder8.run2* directory. By looking at this file, you can see where the mismatches come from. See openbook for more explanation about simCompare.

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