Cadence Tutorial 4

Simulating a Schematic with Verilog-XL

EE577b Spring2000

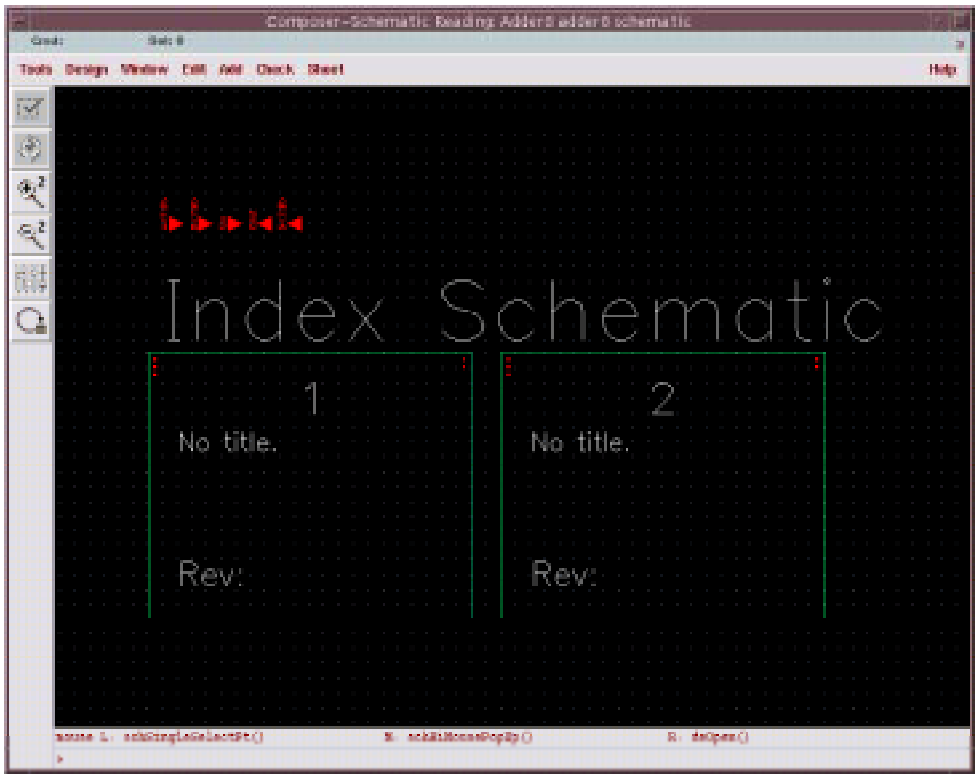
In this tutorial, you will run a Verilog simulation on the schematic cellview of adder8.

1. Tutorial Setup

1. Finish the cadence tutorial 3 before you start this tutorial.
2. Invoke "icfb".

2. Open the 8-bit Adder Schematic Cellview

1. From the Library Manager, read the *adder8 schematic* cellview from the *Adder8* library.
   The *adder8 schematic* cellview is displayed.



3. Initializing Verilog Integration

1. Start Verilog integration by selecting sch : **Tools->Simulation->Verilog-XL** from the *adder8 schematic* cellview.
   The Verilog-XL Setup Environment window is displayed.

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2. In the Verilog-XL Setup Environment window, enter *adder8.run2* for the run directory. All other default values are correct.
3. Click on OK.

   The Verilog-XL Integration control window is opened. The *adder8.run2* run directory is created and the environment is initialized.

4. Setting the Netlist and Waveform Options

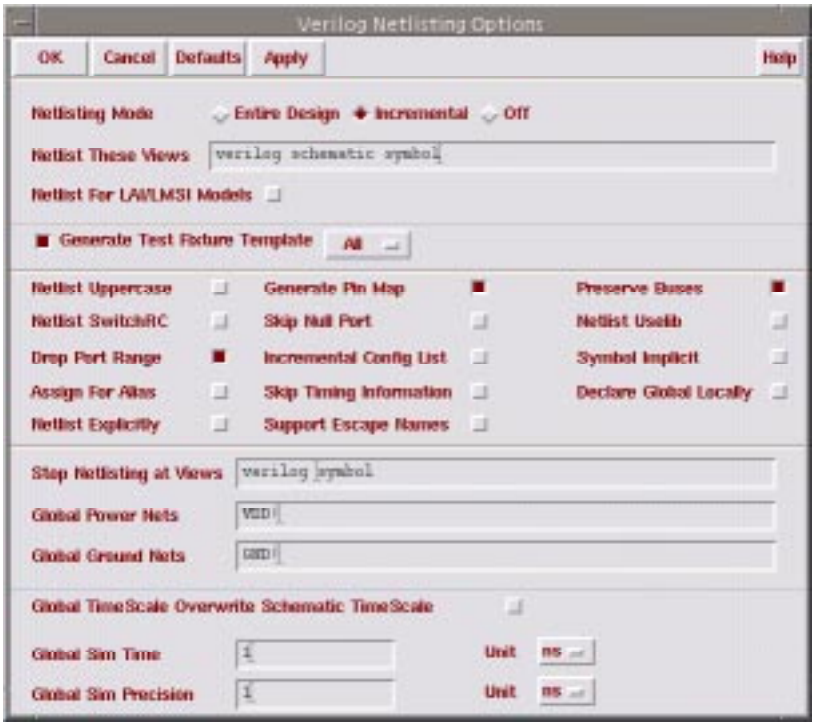
1. In the Verilog-XL window, set the Netlisting Options by selecting **Setup->Netlist**.

   The Netlisting Options form is displayed.
2. In the Netlisting Option window, set **Netlist These Views** list to:

   `verilog schematic symbol`
3. Click on **More>>**

   Additional netlisting options are added to the form.
4. Define **Stop Netlisting at Views** as:

   `verilog symbol`
5. Click on **Generate Pin Map** to turn it on.
6. Click on OK.



5. Creating the Stimulus File

The test fixture file used in the previous tutorial is used for this tutorial as well.

1. Create a Test Fixture (Stimulus) file by selecting

   Stimulus->Verilog
2. Click on No on the dialog box that appears to copy test fixture file on *adder8.run1*.
3. Select *testfixture.verilog* file of *adder8.run1* in **Copy From** and click **copy** on Mode.
4. Type *testfixture.verilog* in **Copy To**.
5. Click OK.

   These steps are for copying *testfixture.verilog* of *adder8.run1* to *adder8.run2*.

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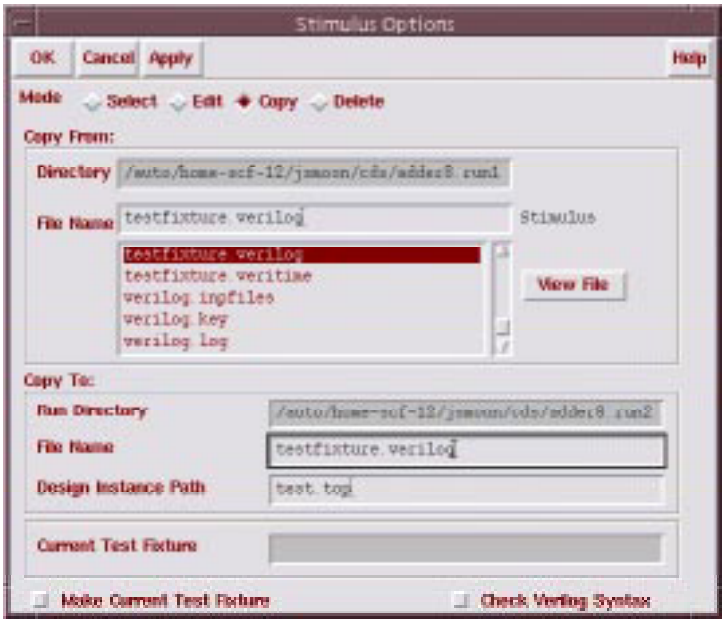

6. Select *testfixture.verilog* by **Stimulus->Verilog** again.
   Click *testfixture.verilog* and click on **Select** at Mode.

6. Simulation

All simulation steps are same as the previous tutorial.
For the compilation of verilog netlist from schematic, you need to include all netlist files in "ihnl" subdirectory. If you finish the generation of netlist from schematic, you should have 8 subdirectories under "ihnl".
In testfixture.template file, please add the lines as follows (modify it according to your running directory).

`include "/home/scf-12/jsmoon/cds/adder8.run2/hdlFilesDir/cds_globals.v"
`include "/home/scf-12/jsmoon/cds/adder8.run2/ihnl/cds0/netlist"
`include "/home/scf-12/jsmoon/cds/adder8.run2/ihnl/cds1/netlist"
`include "/home/scf-12/jsmoon/cds/adder8.run2/ihnl/cds2/netlist"
`include "/home/scf-12/jsmoon/cds/adder8.run2/ihnl/cds3/netlist"
`include "/home/scf-12/jsmoon/cds/adder8.run2/ihnl/cds4/netlist"
`include "/home/scf-12/jsmoon/cds/adder8.run2/ihnl/cds5/netlist"
`include "/home/scf-12/jsmoon/cds/adder8.run2/ihnl/cds6/netlist"

cds_globals.v file is necessary because it has the definition of vdd and gnd.

If you get the following error message when you initiate verilog-xl interactive,

ERROR: hnlCellExtractedC -- Netlister: the cell adder8 was modified since last extraction.

Check & Save the schematic from bottom cell to top-most .. then start
verilog-xl again.

7. Netlist Files

Take a look at the netlist Þles in *ihnl/cds0* directory. You can see how transistor schematic is netlisted in verilog code.

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